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Title: Evaluation of Power Costs in Triplicated FPGA Designs

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Evaluation of Power Costs in Triplicated FPGA Designs

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1 Introduction

Triple modular redundancy (TMR) is a technique commonly used to provide design hardening. Previous studies have shown that a feedback style of TMR[1] will ensure the reliability of designs in the presence of single event upsets (SEUs)[2]. This previous work showed that reliability comes at the cost of at least 3x in design area (sometimes as much as 6x) and at the cost of reduced clock rates. Another, perhaps more important cost consideration is the increase in power consuption due to TMR. This study investigates the cost of TMR in terms of power consumption on different Xilinx FPGA architectures. In this study we use a more classical TMR style rather than the selective feedback style. Xilinx's XPower power estimation tool[3] as well as ISI's SLAAC1V[4] board power measurement tool allow us to accurately estimate and measure the power consumed by various designs. The results of this study show that the choice of FPGA architecture greatly affects the amount of power consupmtion. The study also shows that design placement also affects how much power is consumed.

2 Power Measurement and Estimation Callibration

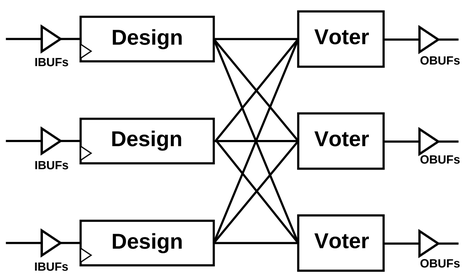
JPower

- Current measuring tool for the SLAAC1V Board (Virtex only)
- Tool made functional at LANL by Jared Zimmerman
- 2.5 V channel sampled at 120 kHz
- Current stored as 10-bit number then multiplied by 4.8828125 mA
- Current measurements up to 4990 mA

XPower

- Xilinx power measurement tool
- ModelSim *.vcd files and timing information required

Classic TMR

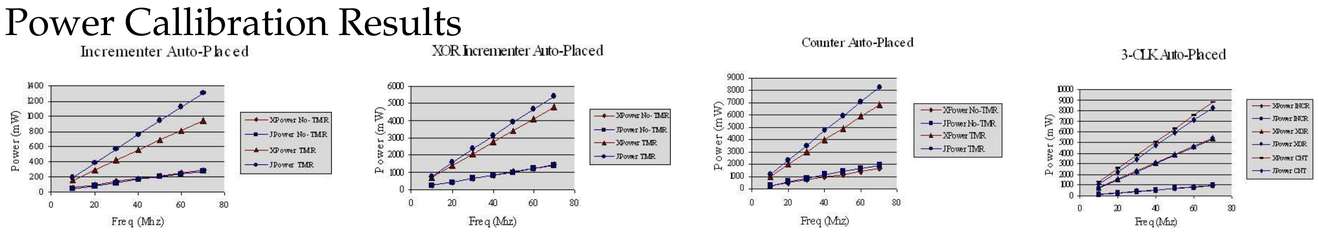


- TMR applied at top level
- Top level IBUFs and OBUFs also triplicated
- Our studies used this style of TMR

Callibration Designs

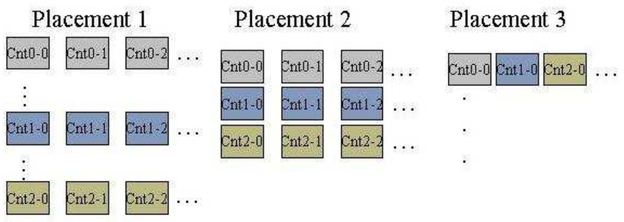
- **72 Incrementers** - each output leading to an IOB
- **416 Incrementers** - outputs grouped into **XOR** gates leading to IOBs
- **416 Up/down loadable counters** - final counter output leading to IOBs
- The above 3 designs but with **triplicated clocks**

Power Callibration Results



	Non-TMR			Classic TMR			3 CLK (TMR)		
	INC	XOR	CNT	INC	XOR	CNT	INC	XOR	CNT
Frequency vs. Power Slopes									
JPower	1.54	7.85	11.08	7.37	31.13	47.53	5.37	30.67	48.14
XPower	1.54	7.95	9.26	5.23	27.06	39.03	5.28	30.62	49.94
Area Costs									
LUTs	576	3250	3328	1728	9750	19968	1728	9750	19968

3 Effects of Placement on Power Consumption



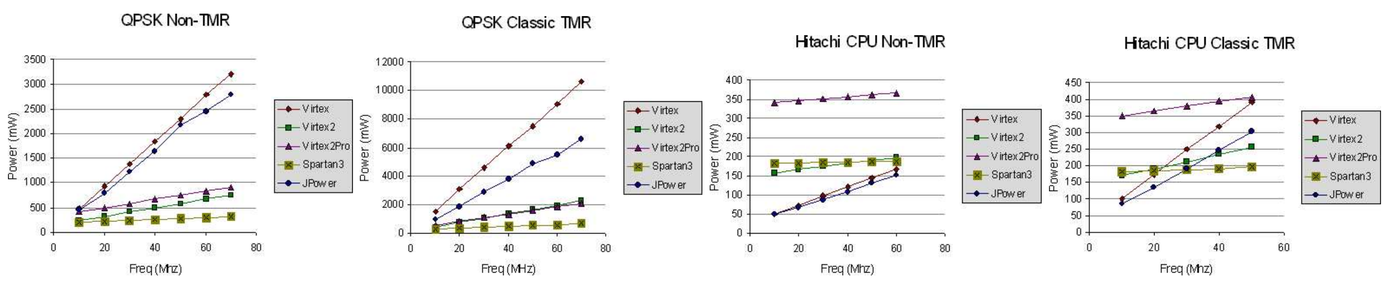
- Placement studies primarily done on **72 incrementer** design
- Xilinx auto-placement and 3 hand placements considered
- Only auto-placement and one hand placement considered for other designs

	Incrementer			
	Auto-Place	Place 1	Place 2	Place 3
Frequency vs. Power Slopes (TMR)				
JPower	7.37	10.65	6.15	4.76
XPower	5.23	6.20	5.21	4.78
Power Increase Due to TMR				
JPower	4.79x	7.04x	4.06x	3.15x
XPower	3.40x	4.04x	3.39x	3.10x

	Incrementer		XOR Incrementer		Up/Down Counter	
	Auto-Place	Hand-Place	Auto-Place	Hand-Place	Auto-Place	Hand-Place
Frequency vs. Power Slopes						
JPower	7.37	4.78	31.13	22.18	47.53	41.22
XPower	5.23	4.76	27.06	25.10	39.03	36.40
JP / XP	1.41	1.00	1.15	0.88	1.22	1.13

4 Power Costs of Realistic Designs on Different Xilinx Architectures

Power Consumption Results



	Non-TMR					TMR				
	JPower	Virtex	Virtex2	Virtex2Pro	Spartan3	JPower	Virtex	Virtex2	Virtex2Pro	Spartan3
Frequency vs. Power Slopes										
QPSK	40.50	45.71	8.60	8.16	1.97	93.75	150.64	30.17	24.98	6.68
Hitachi	2.06	2.34	0.79	0.48	0.12	5.48	7.30	2.10	1.39	0.30

		QPSK Demodulator	Hitachi CPU
Virtex	**TMR Area Cost**	3.03x	3.01x
	TMR Speed Cost	95.2%	71.1%
	TMR Power Cost	3.30x	3.12x
Virtex2	**TMR Area Cost**	3.03x	3.00x
	TMR Speed Cost	84.6%	100.0%
	TMR Power Cost	3.51x	2.66x
Virtex2Pro	**TMR Area Cost**	3.03x	3.00x
	TMR Speed Cost	77.9%	80.8%
	TMR Power Cost	3.06x	2.88x
Spartan3	**TMR Area Cost**	3.02x	3.00x
	TMR Speed Cost	97.2%	87.0%
	TMR Power Cost	3.39x	2.50x

5 Conclusion

- Power increase to TMR is 3x (can be more with poor design placement)
- FPGA architecture significantly affects power consumption

References

[1] Carl Carmichael. Triple module redundancy design techniques for Virtex FPGAs. Technical report, Xilinx Corporation, November 1, 2001. XAPP197 (v1.0).

[2] Nathan Rollins, Michael Wirthlin, Michael Caffrey, and Paul Graham. Evaluating tmr techniques in the presence of single event upsets. In *Proceedings of the 6th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, September 2003. To Be Published.

[3] Xilinx, Inc. *XPower Manual*.

[4] USC-ISI East. *SLAAC-1V User VHDL Guide*, October 1, 2000. Release 0.3.1.